DIGITALLY ADJUSTABLE LCD BOOST CONVERTER

FEATURES

- **Input Voltage Range . . . 1.8 V to 6.0 V**
- **Up to 85% Efficiency**
- **Digitally Adjustable Output Voltage Control**
- **Disconnects Output From Input During Shutdown**
- **Switching Frequency . . . Up to 1 MHz**
- **No Load Quiescent Current . . . 40 µA Typ**
- **Thermal Shutdown Mode**
- **Shutdown Current . . . 0.1 µA Typ**
- **Available in Small 3mm × 3mm QFN package**

APPLICATIONS

- **LCD Bias Supply For Small to Medium LCD Displays**
- **OLED Display Power Supply**
  - **– PDA, Pocket PC, Smart Phones**
  - **– Handheld Devices**
  - **– Cellular Phones**

DESCRIPTION

The TPS61045 is a high frequency boost converter with digitally programmable output voltage and true shutdown. During shutdown the output is disconnected from the input by opening the internal input switch. This allows a controlled power up/down sequencing of the display. The output voltage can be increased or decreased in digital steps by applying a logic signal to the CTRL pin. The output voltage range, as well as the output voltage step size, can be programmed with the feedback divider network. With a high switching frequency of up to 1 MHz the TPS61045 allows the use of small external components and together, with the small 8-pin QFN package, a minimum system solution size is achieved.

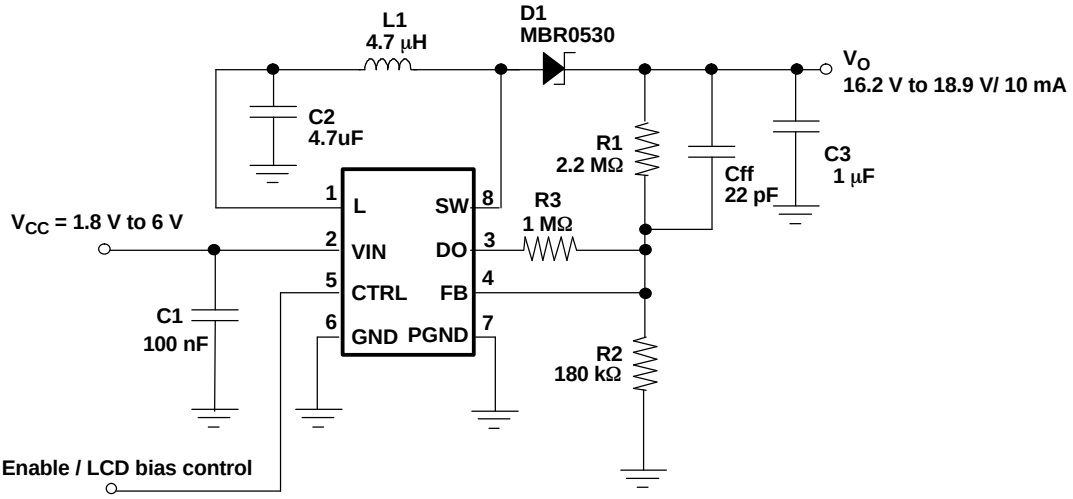

Figure 1. Typical Application

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	8 Pin QFN Package (DRB)	Package Marking
-40°C to 85°C	TPS61045DRB	BHT

(1) The DRB package is available taped and reeled. Add R suffix (TPS61045DRBR) to order quantities of 3000 units per reel. Add T suffix (TPS61045DBRT) to order quaqntities of 250 units per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	TPS61045
Supply voltage, $V_{(VIN)}$(2)	-0.3 V to 7 V
Voltages, $V_{(CTRL)}$, $V_{(FB)}$, $V_{(L)}$, $V_{(DO)}$(2)	-0.3 V to V_I + 0.3 V
Voltage, $V_{(SW)}$(2)	30 V
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range	-40° C to 150° C
Storage temperature range, T_{STG}	-65° C to 150° C
Lead temperature (soldering, 10 sec)	260° C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
8 pin QFN (DRB) (1)	370 mW	3.7 mW/° C	204 mW	148 mW

(1) The thermal resistance junction to ambient of the 8 pin QFN package is 270°C/W. Standard 2 layer PCB without vias for the thermal pad. See the appliction section on how to improve the thermal resistance $R_{\Theta JA}$.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
$V_{(VIN)}$	Input voltage range	1.8		6.0	V
$V_{(SW)}$	Switch voltage			30	V
L	Inductor (1)		4.7		µH
f	Switching frequency(1)			1	MHz
$C_{I(C2)}$	Input capacitor (C2) (1)		4.7		µF
$C_{O(C3)}$	Output capacitor (C3) (1)		1		µF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

(1) See application section for further information.

ELECTRICAL CHARACTERISTICS

V_I = 2.4 V, CTRL = V_I, V_O = 18.0 V, I_O = 10 mA, T_A = -40°C to 85°C, typical values are at T_A = 25° C (unless otherwise noted)

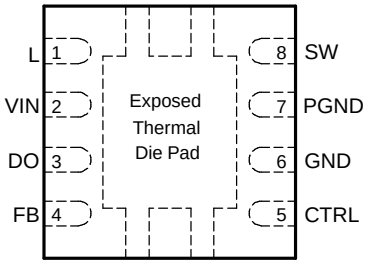
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current						
V_I	Input voltage range		1.8		6.0	V

ELECTRICAL CHARACTERISTICS (continued)

V_I = 2.4 V, CTRL = V_I, V_O = 18.0 V, I_O = 10 mA, T_A = -40°C to 85°C, typical values are at T_A = 25° C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Operating quiescent current	I_O = 0 mA, not switching		40	65	µA
$I_{O(SD)}$	Shutdown current	CTRL = GND		0.1	1	µA
V_{UVLO}	Under-voltage lockout threshold	V_I falling		1.5	1.7	V
CTRL and DAC output						
V_{IH}	CTRL high level input voltage		1.3			V
V_{IL}	CTRL low level input voltage				0.3	V
I_{lkg}	CTRL input leakage current	CTRL = GND or VIN			0.1	µA
$V_{O(DO)}$	DAC output voltage range		0		1.233	V
	DAC resolution	6 Bit		19.6		mV
$V_{O(DO)}$	DAC center output voltage	CTRL = high		607		mV
$I_{O(SINK)}$	Maximum DAC sink current				30	µA
$t_{(UP)}$	Increase output voltage one step	CTRL = high to low	1		60	µs
$t_{(DWN)}$	Decrease the output voltage one step	CTRL = high to low	140		240	µs
t_{d1}	Delay time between up/down steps	CTRL = low to high	1			µs
$t_{(OFF)}$	Shutdown	CTRL = high to low	560			µs
Input switch (Q1), main switch (Q2) and current limit						
$V_{SW(Q2)}$	Main switch maximum voltage (Q2)				30	V
$r_{ds(ON)}$	Main switch MOSFET on-resistance	V_I = 2.4 V; I_S = 200 mA		400	800	mΩ
$I_{lkg(MAIN)}$	Main switch MOSFET leakage current	V_S = 28 V		0.1	10	µA
$I_{(LIM)}$	Main switch MOSFET current limit		300	375	450	mA
$r_{ds(ON)}$	Input switch MOSFET on-resistance	V_I= 2.4 V; I_S = 200 mA		1	2	Ω
$I_{lkg(IN)}$	Input switch MOSFET leakage current	VL = GND, V_I = 6 V		0.1	10	µA
Output						
V_O	Output voltage range		Vin		28	V
V_{ref}	Internal voltage reference			1.233		V
$I_{(FB)}$	Feedback input bias current	VFB = 1.3 V		30	100	nA
$V_{(FB)}$	Feedback trip point voltage	1.8 V ≤ V_I≤ 6.0 V; V_O = 18 V, $I_{(LOAD)}$= 10 mA	1.208	1.233	1.258	V

DRB PACKAGE
(TOP VIEW)

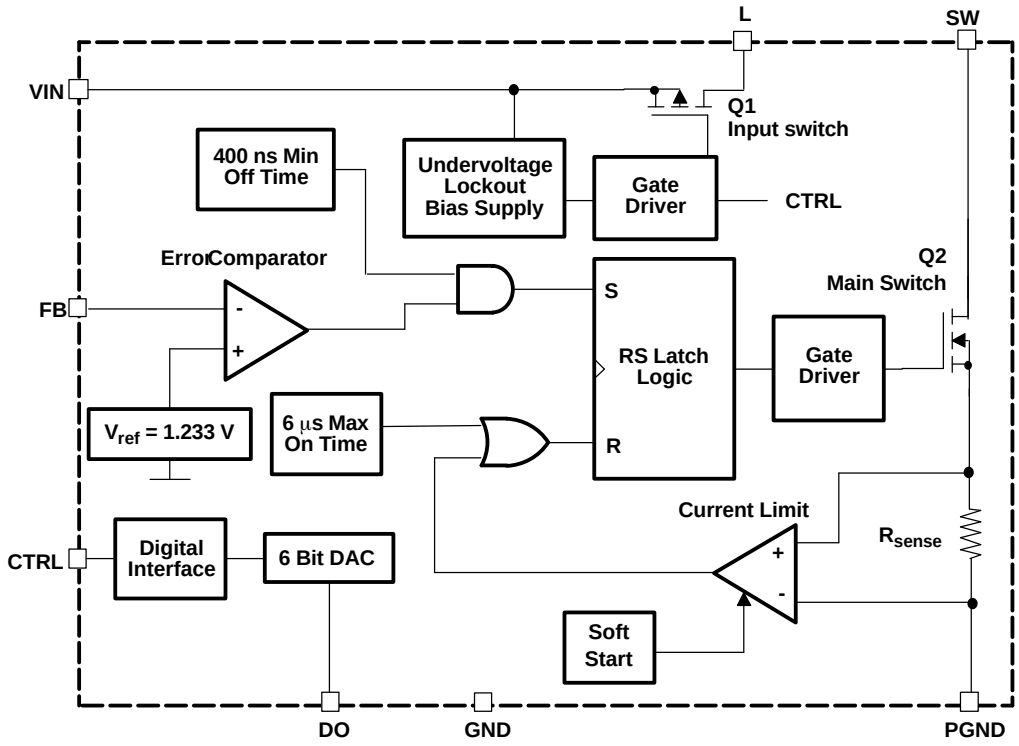


The Exposed Thermal Die Pad is connected to PGND. Connect this pad directly with the GND pin.

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CTRL	5	I	Combined enable and digital output voltage programming pin. Pulling CTRL constantly high enables the device. When CTRL is pulled to GND, the device is disabled and the input is disconnected from the output by opening the integrated switch Q1. Pulsing CTRL low increases or decreases the output voltage. Refer to the *application information* section for further information.
DO	3	O	Internal DAC output. DO programs the output voltage via the CTRL pin. Refer to the *application information* section for further information.
FB	4	I	Feedback. FB must be connected to the output voltage-feedback divider.
GND	7		Analog ground. GND must be directly connected to the PGND pin. Refer to the *application information* section for further information.
L	1	O	Drain of the internal switch (Q1). Connect L to the inductor.
PGND	6		Power ground
SW	8	I	Drain of the integrated switch Q2. SW is connected to the inductor and anode of the Schottky rectifier diode.
VIN	2	I	Input supply pin

FUNCTIONAL BLOCK DIAGRAM



Typical Characteristics

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	Figure 2
		vs Input voltage	Figure 3
$I_{DD(Q)}$	Quiescent current	vs Input voltage	Figure 4
$V_{(FB)}$	Feedback voltage	vs Temperature	Figure 5

Typical Characteristics (continued)

Table of Graphs (continued)

			FIGURE
$I_{(FB)}$	Feedback current	vs Temperature	Figure 6
$r_{ds(on)}$	$r_{ds(on)}$ Main switch Q2	vs Temperature	Figure 7
		vs Input voltage	Figure 8
	$r_{ds(on)}$ Input switch Q1	vs Temperature	Figure 9
		vs Input voltage	Figure 10
$V_{(DO)}$	$V_{(DO)}$ Voltage	vs CTRL input step	Figure 11
	Line transient response		Figure 12
	Load transient response		Figure 13
	PFM operation		Figure 14
	Soft start		Figure 15

Efficiency vs Load Current

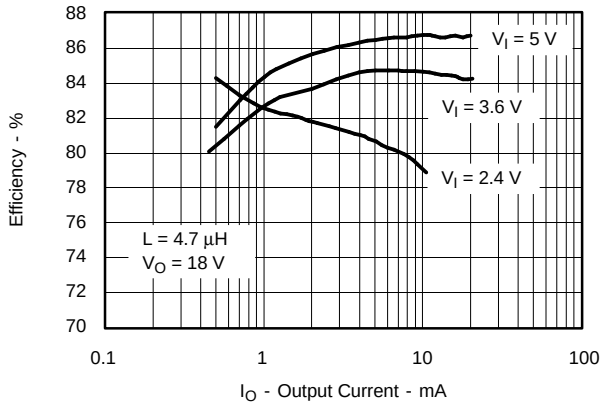


Figure 2.

Efficiency vs Input Voltage

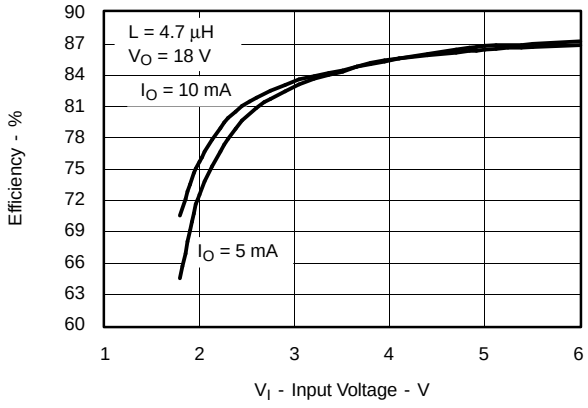


Figure 3.

Quiescent Current vs Input Voltage

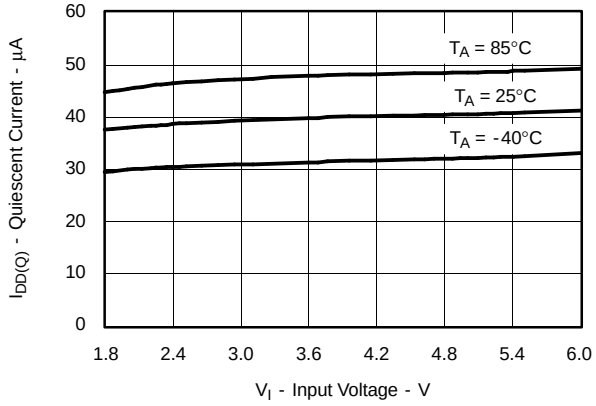


Figure 4.

Feedback Voltage vs Temperature

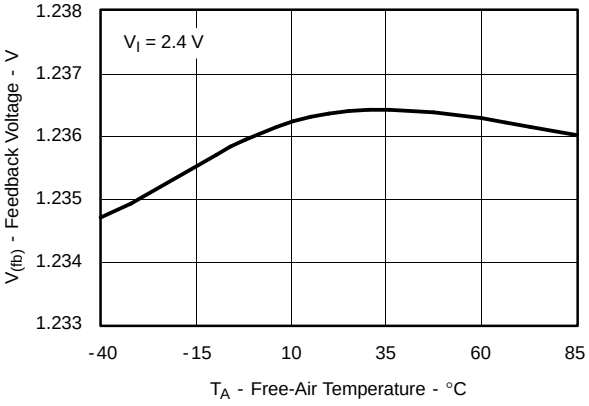


Figure 5.

Feedback Current vs Temperature

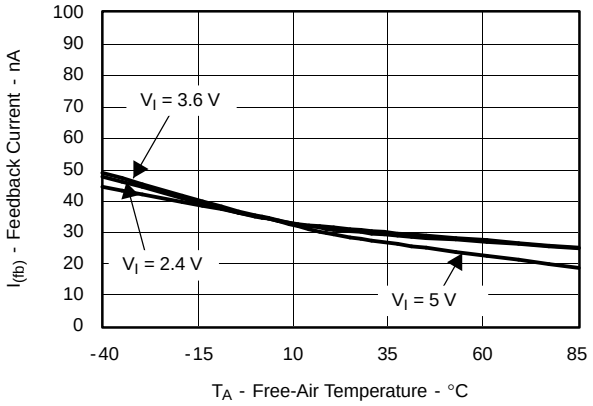


Figure 6.

$r_{ds(ON)}$ Main Switch Q2 vs Temperature

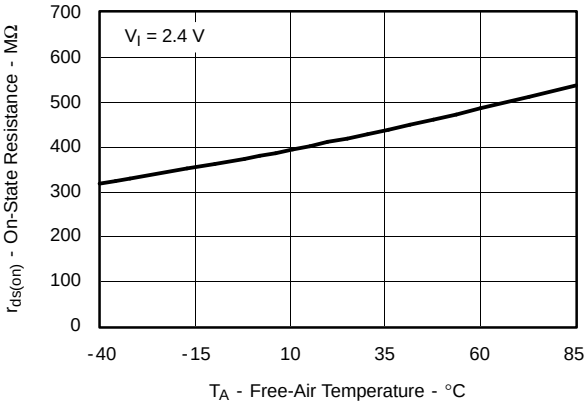


Figure 7.

$r_{ds(ON)}$ Main Switch Q2 vs Input Voltage

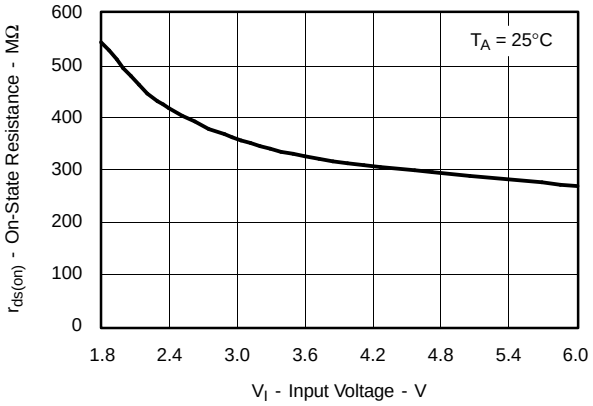


Figure 8.

$r_{ds(ON)}$ Input Switch Q1 vs Temperature

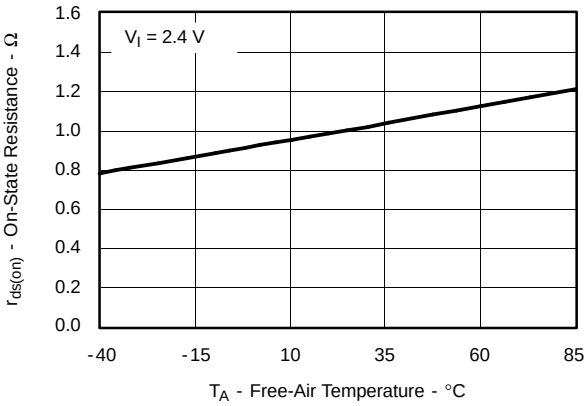


Figure 9.

$r_{ds(ON)}$ Input Switch Q1 vs Input Voltage

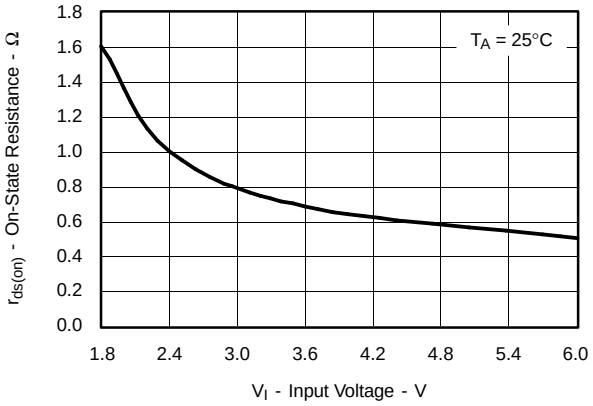


Figure 10.

$V_{(DO)}$ Voltage vs CTRL Input Step

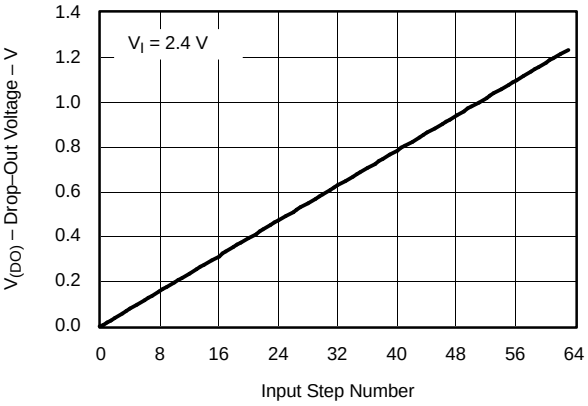


Figure 11.

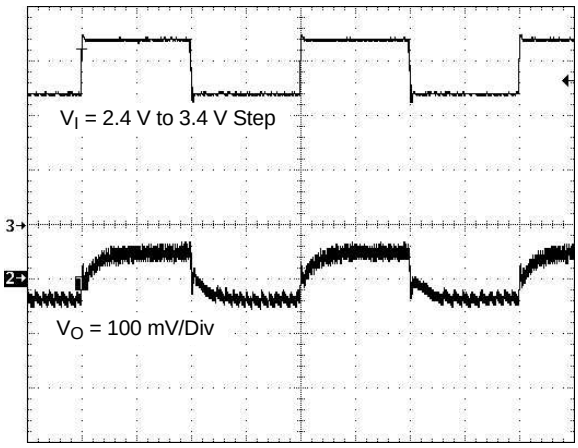


Figure 12. . Line Transient Response

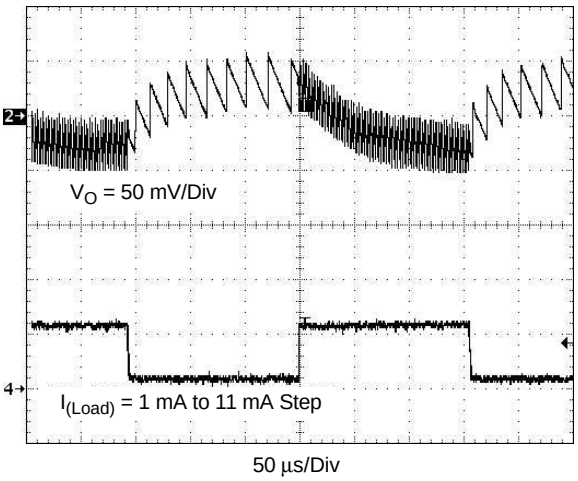


Figure 13. . Load Transient Response

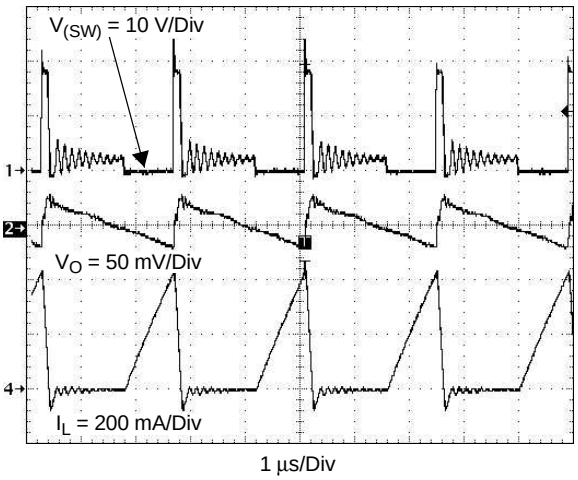


Figure 14. . PFM Operation

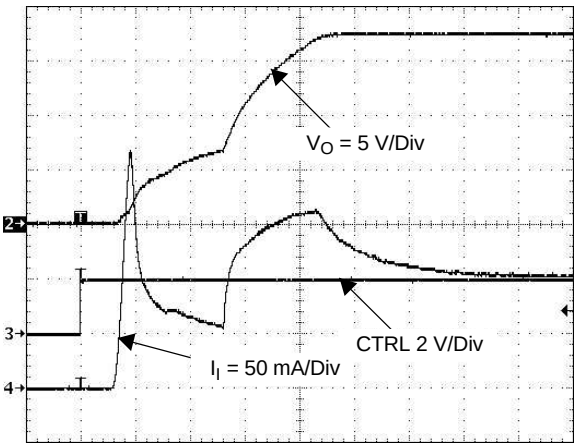


Figure 15. . Soft Start

DETAILED DESCRIPTION

OPERATION

The TPS61045 operates with an input voltage range of 1.8 V to 6.0 V and generates output voltages up to 28 V. The device operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and, with a switching frequency of up to 1 MHz, the device enables the use of small external components.

The converter monitors the output voltage and when the feedback voltage falls below the reference voltage of 1.233 V (typ) the main switch turns on and the current ramps up. The main switch turns off when the inductor current reaches the internally set peak current of 375 mA (typ). Refer to the *peak current control*section for more information. The second criteria that turns off the main switch is the maximum on-time of 6 µs (typ). This limits the maximum on-time of the converter in extreme conditions. As the switch is turned off, the external Schottky diode is forward biased delivering the current to the output. The main switch remains off until the minimum off time of 400 ns (typ) has passed and the feedback voltage is below the reference voltage again. Using this PFM peak current control scheme, the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the input voltage, output voltage and output current. This gives a high efficiency over the entire load current range. This regulation scheme is inherently stable which allows a wider range for the selection of the inductor and output capacitor.

PEAK CURRENT CONTROL

The internal switch is turned on until the inductor current reaches the typical dc current limit (I_{LIM}) of 375 mA. Due to the internal current limit delay of 100 ns (typ) the actual current exceeds the dc current limit threshold by a small amount. The typical peak current limit can be calculated:

$$I_{P(typ)} = I_{(LIM)} + \frac{V_I}{L} \times 100\ ns$$

$$I_{P(typ)} = 400\ mA + \frac{V_I}{L} \times 100\ ns$$

The higher the input voltage and the lower the inductor value, the greater the current limit overshoot.

SOFTSTART

All inductive step-up converters exhibit high inrush current during start up if no special precautions are taken. This can cause voltage drops at the input rail during start-up, which may result in an unwanted or premature system shut down.

DETAILED DESCRIPTION (continued)

When the device is enabled, the internal input switch (Q1) is slowly turned on to reduce the in-rush current charging the capacitor (C2) connected to pin L. Furthermore, the TPS61045 limits this in-rush current during start-up by increasing the current limit in two steps starting from $I_{LIM}/4$ for 256 switch cycles to $I_{LIM}/2$ for the next 256 switch cycles.

ENABLE (CTRL PIN)

The CTRL pin serves two functions. One is the enable and disable of the device. The other is the output voltage programming of the device. If the digital interface is not required, the CTRL pin is used as a standard enable pin for the device.

Pulling the CTRL pin high enables the device beginning with the softstart cycle.

Pulling the CTRL pin to ground for a period of ≥ 560 µs shuts down the device, reducing the shutdown current to 0.1 µA (typ). During shutdown the internal input switch (Q1) remains open and disconnects the load from the input supply of the device.

This pin must be terminated.

DAC OUTPUT (DO)

The TPS61045 allows digital adjustment of the output voltage using the digital CTRL interface as described in the next section. The DAC output pin (DO) drives an external resistor (R3) connected to the external feedback divider. The DO output has a typical output voltage range from 0 V to V_{ref} (1.233V). If the DO output voltage is set to 0 V, the external resistor (R3) is more or less in parallel to the lower feedback resistor (R2) giving the highest output voltage. Programming the DO output to V_{ref} gives the lowest output voltage. Internally, a 6-bit DAC is used with 64-steps and 0 as the first step. This gives a typical voltage step of 19.6 mV which is calculated as:

$$\left(V_{O(DO)} = \frac{V_{ref}}{2^6 - 1}\right)$$

See the section*setting the output voltage* for further information.

After start-up, when the CTRL pin is pulled high, the DO output voltage is set to its center voltage which is the 32nd step of typically $V_{(DO)}$ = 607mV.

DIGITAL INTERFACE (CTRL)

When the CTRL pin is pulled high the device starts up with softstart and the DAC output voltage (DO) sets to its center voltage with a typical output voltage of 607 mV.

The output voltage can be programmed by pulling the CTRL pin low for a certain period of time. Depending on this time period the internal DAC voltage increases or decreases one digital step, as outlined in Table 1 and Figure 16. Programming the DAC output $V_{(DO)}$ to 0 V places R3 in parallel to R2, which gives the maximum output voltage. If the DAC is programmed to its maximum output voltage equal to the internal reference voltage, typically $V_{(DO)}$=1.233 V, then the output has its minimum output voltage.

DETAILED DESCRIPTION (continued)

Table 1. Timing Table

DAC OUTPUT DO	TIME	LOGIC LEVEL
Increase one step	$t_{(UP)}$ = 1 µs to 60 µs	Low
Decrease one step	$t_{(DWN)}$ = 140 µs to 240 µs	Low
Shutdown	$t_{(OFF)} \geq$ 560 µs	Low
Delay between steps	t_{d1} = 1 µs	High

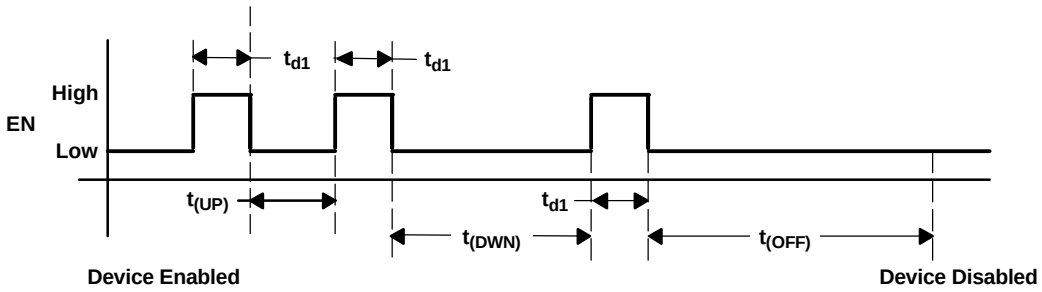


Figure 16. CTRL Timing Diagram

UNDERVOLTAGE LOCKOUT

An undervoltage lockout feature prevents misoperation of the device at input voltages below 1.5 V (typ). As long as the input voltage is below the undervoltage threshold the device remains off, with the input switch (Q1) and the main switch (Q2) open.

THERMAL SHUTDOWN

An internal thermal shutdown is implemented in the TPS61045 that shuts down the device if the typical junction temperature of 160°C is exceeded. If the device is in thermal shutdown mode, the input switch (Q1) and the main switch (Q2) are open.

APPLICATION INFORMATION

INDUCTOR SELECTION, MAXIMUM LOAD CURRENT

Since the PFM peak current control scheme is inherently stable the inductor and capacitor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input, and output voltage of the application determines the switching frequency of the converter. Depending on the application, inductor values between 2.2 µH up to 47 µH are recommended. The maximum inductor value is determined by the maximum switch on-time of 6 µs (typ). The peak current limit of 375 mA (typ) must be reached within this 6 µs for proper operation.

The inductor value determines the maximum switching frequency of the converter. Therefore, the inductor value must be selected for the maximum switching frequency, at maximum load current of the converter and should not be exceeded. A good inductor value to start with is 4.7 µH. The maximum switching frequency is calculated as:

$$f_{s(max)} = \frac{V_I \times \left(V_O - V_I\right)}{I_P \times L \times V_O}$$

with:

I_P = peak current as described in the previous *peak current control* section.

$$I_{P(typ)} = 375\ mA + \frac{V_I}{L} \times 100\ ns$$

L = selected inductor value

If the selected inductor does not exceed the maximum switching frequency of the converter, as a next step, the switching frequency at the nominal load current is estimated as follows:

$$f_{s(ILOAD)} = \frac{2 \times I_{LOAD} \times \left(V_O - V_I + V_F\right)}{I_P^2 \times L}$$

with:

I_P = peak current as described in the previous *chapter peak current control* section

$$I_{P(typ)} = 375\ mA + \frac{V_I}{L} \times 100\ ns$$

L = selected inductor value

$I_{(LOAD)}$ = nominal load current

V_F = rectifier diode forward voltage (typically 0.3 V)

The smaller the inductor value, the higher the switching frequency of the converter but the lower the efficiency.

The maximum load current of the converter is determined at the operation point where the converter starts to enter continuous conduction mode. The converter must always operate in discontinuous conduction mode to maintain regulation.

Two conditions exist for determining the maximum output current of the converter. One is when the inductor current fall time is <400 ns, and the other is when the inductor current fall time is >400 ns.

One way to calculate the maximum available load current under certain operation conditions is to estimate the expected converter efficiency at the maximum load current. This number can be taken out of the efficiency graphs shown in Figure 2 and Figure 3. Then the maximum load current can be estimated:

Inductor fall time:

APPLICATION INFORMATION (continued)

$$t_{fall} = \frac{I_P \times L}{V_O - V_I}$$

For $t_f \geq 400$ ns

$$I_{load\ max} = \eta \frac{I_P \times V_I}{2 \times V_O}$$

$t_f \leq 400$ ns

$$I_{load\ max} = \eta \times \frac{I_P^2 \times L \times V_I}{\left(V_O - V_I\right) \times \left(2 \times I_P \times L + 2 \times 400\ ns \times V_I\right)}$$

with:

L = selected inductor value

η = expected converter efficiency (typically between 70% to 85%)

I_P = peak current as described in the previous *peak current control* section.

$$I_P = 300\ mA + \frac{V_I}{2} \times 100\ ns$$

The above formula contains the expected converter efficiency that allows calculating the expected maximum load current the converter can support. The efficiency can be taken out of the efficiency graphs shown in Figures 2 and 3 or 80% can be used as a good estimation.

The selected inductor must have a saturation current which meets the maximum peak current of the converter as calculated in the *peak current control* section. Use the maximum value for I_{Lim} (450mA) for this calculation.

Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter. Refer to the Table 1 and the *inductor selection* section under *typical applications*.

Table 2. Possible Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
10 µH	Sumida CR32-100	High efficiency
10 µH	Sumida CDRH3D16-100	High efficiency
10 µH	Murata LQH43CN100K01	
4.7 µH	Sumida CDRH3D16-4R7	Small solution size
4.7 µH	muRata LQH32CN4R7M51	Small solution size

SETTING THE OUTPUT VOLTAGE

When the converter is programmed to the minimum output voltage, the DAC output (DO) equals the reference voltage of 1.233 V (typ). Therefore, only the feedback resistor network (R1) and (R2) determines the output voltage under these conditions. This gives the minimum output voltage possible and can be calculated as:

$$V_{O(min)} = V_{(FB)} \times \left(\frac{R1}{R2} + 1\right)$$

The maximum output voltage is determined as the DAC output (DO) is set to 0 V:

$$V_{O(max)} = V_{(FB)} \times \frac{R1}{R3} + V_{(FB)} \times \left(\frac{R1}{R2} + 1\right)$$

The output voltage can be digitally programmed by pulling the CTRL pin low for a certain period of time as described in the *Digital Interface* section. Pulling the signal applied to the CTRL pin low increases or decreases the DAC output DO (pin 3) one-step where one step is typically 19.6 mV. A voltage step on DO of 19.6mV (typ) changes the output voltage by one step and is calculated as:

$$V_{O(step)} = \frac{19.6\ mV \times R1}{R3}$$

The possible output voltage range is determined by selecting R1, R2 and R3. A possible larger output voltage range gives a larger output voltage step size. The smaller the possible output voltage range, the smaller the output voltage step size.

To reduce the overall operating quiescent current in battery powered applications a high impedance voltage divider must be used with a typical value for R2 of ≤ 200 kΩ and a maximum value for R1 of 2.2 MΩ.

Some applications may not need the digital interface to program the output voltage. In this case the output DO can be left open as shown in Figure 18 and the output voltage is calculated as for any standard boost converter:

$$V_O = 1.233\ V \times \left(1 + \frac{R1}{R2}\right)$$

In such a configuration a high impedance voltage divider must also be used to minimize ground current and a typical value for R2 of ≤ 200 kΩ and a maximum value for R1 of 2.2 MΩ are recommended.

A feed-forward capacitor ($C_{(FF)}$), across the upper feedback resistor (R1), is required to provide sufficient overdrive for the error comparator. Without a feed-forward capacitor or a too small feed-forward capacitor value, the device shows double pulses or a pulse burst instead of single pulses at the switch node (SW). This can cause higher output voltage ripple. If a higher output voltage ripple is acceptable, the feedforward capacitor can be left out too.

The lower the switching frequency of the converter, the larger the feed-forward capacitor value needs to be. A good starting point is the use of a 10 pF feed-forward capacitor. As a first estimation, the required value for the feed-forward capacitor can be calculated at the operation point:

$$C_{FF} \approx \frac{1}{2 \times \pi \times \frac{f_S}{20} \times R1}$$

with:

R1 = upper resistor of voltage divider

f_S = switching frequency of the converter at the nominal load current. (For the calculation of the switching frequency see previous section)

For $C_{(FF)}$ choose a value which comes closest to the calculation result.

The larger the feed-forward capacitor, the worse the line regulation of the device. Therefore, the feed-forward capacitor must be selected as small as possible if good line regulation is of concern.

OUTPUT CAPACITOR SELECTION

For better output voltage filtering a low ESR output capacitor is recommended. Ceramic capacitors have low ESR values but depending on the application, tantalum capacitors can also be used. Refer to Table 2 and *typical applications* for the selection of the output capacitor.

Assuming the converter does not show double pulses or pulse bursts on the switch node (SW) the output voltage ripple is calculated as:

$$\Delta V_O = \frac{I_O}{C_O} \times \left(\frac{1}{f_{s(ILOAD)}} - \frac{I_P \times L}{V_O + V_F - V_I}\right) + I_P \times ESR$$

with:

I_P = peak current as described in the previous section *peak current control*

$$I_P = 375\ mA + \frac{V_I}{2} \times 100\ ns$$

L = selected inductor value

$I_{O(LOAD)}$=Nominal load current

$f_{S(ILoad)}$ = switching frequency at the nominal load current as calaculated previously.

V_F = rectifier diode forward voltage (typically 0.3 V)

C_O = selected output capacitor

ESR = output capacitor ESR value

INPUT CAPACITOR SELECTION

The input capacitor (C1) filters the high frequency noise to the control circuit and must be directly connected to the input pin (VIN) of the device. The capacitor (C2) connected to the L pin of the device is the input capacitor for the power stage.

The main purpose of the capacitor (C2), that is connected directly to the L pin, is to smooth the inductor current. A larger capacitor reduces the inductor ripple current present at the L pin. The smaller the ripple current at the L pin, the higher the efficiency of the converter. If a sufficiently large capacitor is used, the input switch must carry only the DC current, filtered by the capacitor (C2), and not the high switching currents of the converter. A 4.7 µF or 10-µF ceramic capacitor (C2) is sufficient for most applications. For better filtering, this value can be increased without limit. Refer to Table 2 and *typical applications* for input capacitor recommendations.

Table 3. Possible Input and Output Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMMENTS
4.7 F/X5R/0805	6.3 V	Tayo Yuden JMK212BY475MG	C_I/C_O
10 µF/X5R/0805	6.3 V	Tayo Yuden JMK212BJ106MG	C_I/C_O
1.0 µF/X7R/1206	25 V	Tayo Yuden TMK316BJ105KL	C_O
1.0 µF/X7R/1206	35 V	Tayo Yuden GMK316BJ105KL	C_O
4.7 µF/X5R/1210	25 V	Tayo Yuden TMK325BJ475MG	C_O

DIODE SELECTION

To achieve high efficiency a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter as it is calculated in the *peak current control* section. Use the maximum value for $I_{(LIM)}$ (450mA) for this calculation. Refer to Table 3 and the *typical applications* for the selection of the Schottky diode.

Table 4. Possible Schottky Diode Selection

COMPONENT SUPPLIER	REVERSE VOLTAGE
ON Semiconductor MBR0530	30 V
ON Semiconductor MBR0520	20 V
ON Semiconductor MBRM120L	20 V
Toshiba CRS02	30 V
Zetex CHZS400	40 V

LAYOUT CONSIDERATIONS

As for all switching power supplies the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully implemented the regulator can show noise problems and duty cycle jitter.

The input capacitor must be placed as close as possible to the input pin for good input-voltage filtering. The inductor and diode must be placed as close as possible to the switch pin (SW) to minimize noise coupling into other circuits. Since the feedback pin and network is a high impedance circuit, the feedback network must be routed away from the inductor.

THERMAL CONSIDERATIONS

The TPS61045 is available in a thermally enhanced QFN package. The package includes a thermal pad, improving the thermal capabilities of the package. See QFN/SON PCB attachment application note (SLUA271).

The thermal resistance junction to ambient ($R_{\Theta JA}$) of the QFN package depends on the PCB layout. By using thermal vias and wide PCB, traces improve thermal resistance ($R_{\Theta JA}$). Under normal operation conditions no PCB vias are required for the thermal pad. However, the thermal pad must be soldered to the PCB.

TYPICAL APPLICATIONS

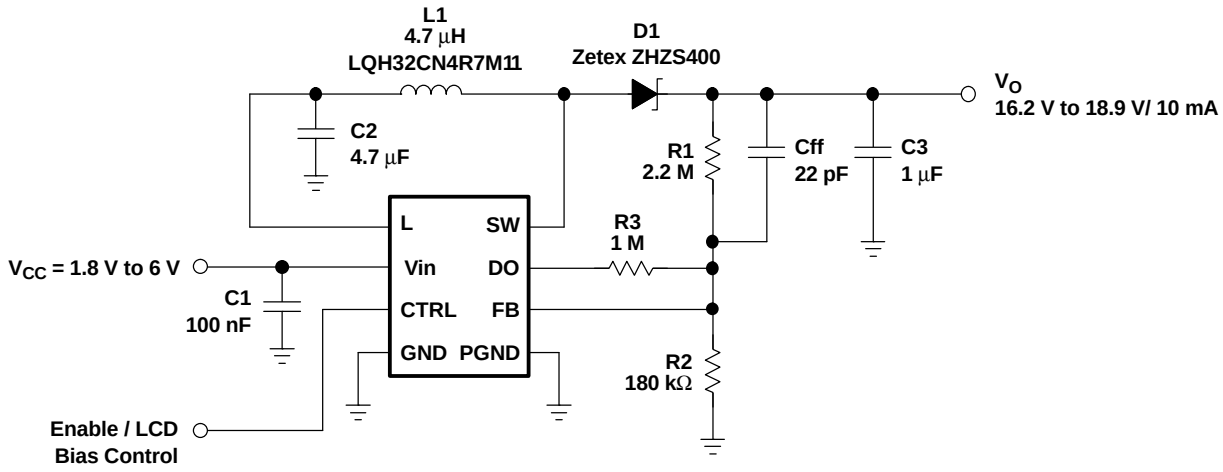


Figure 17. Typical Application With Digital Adjusted Output Voltage

TYPICAL APPLICATIONS (continued)

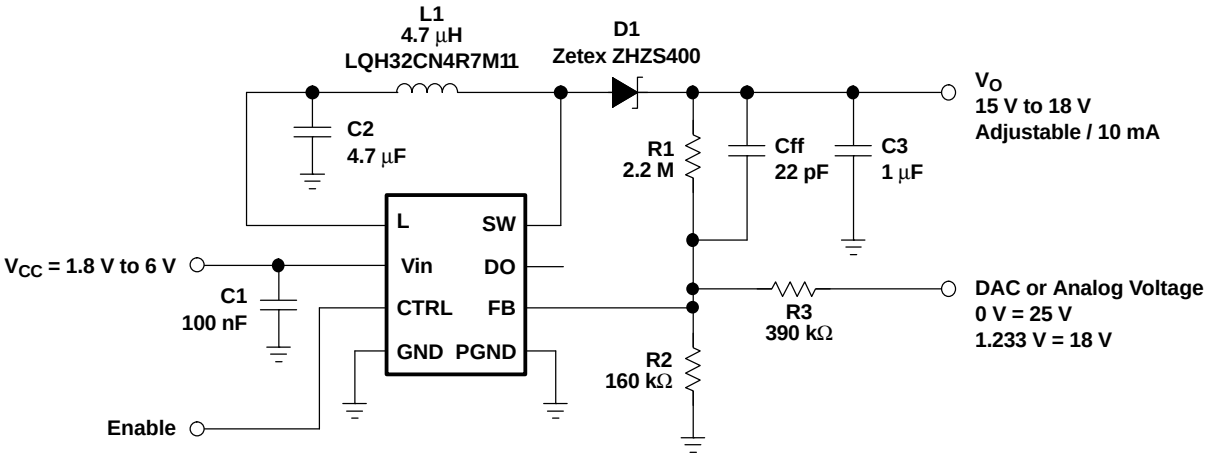


Figure 18. Typical Application With Analog Adjusted Output Voltage

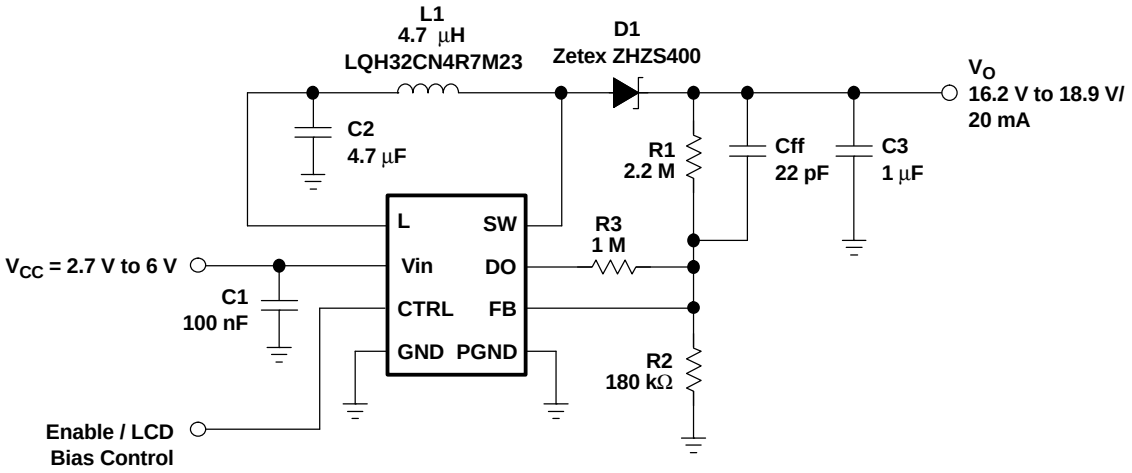


Figure 19. OLED Supply Providing Higher Output Current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS61045DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61045DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61045DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61045DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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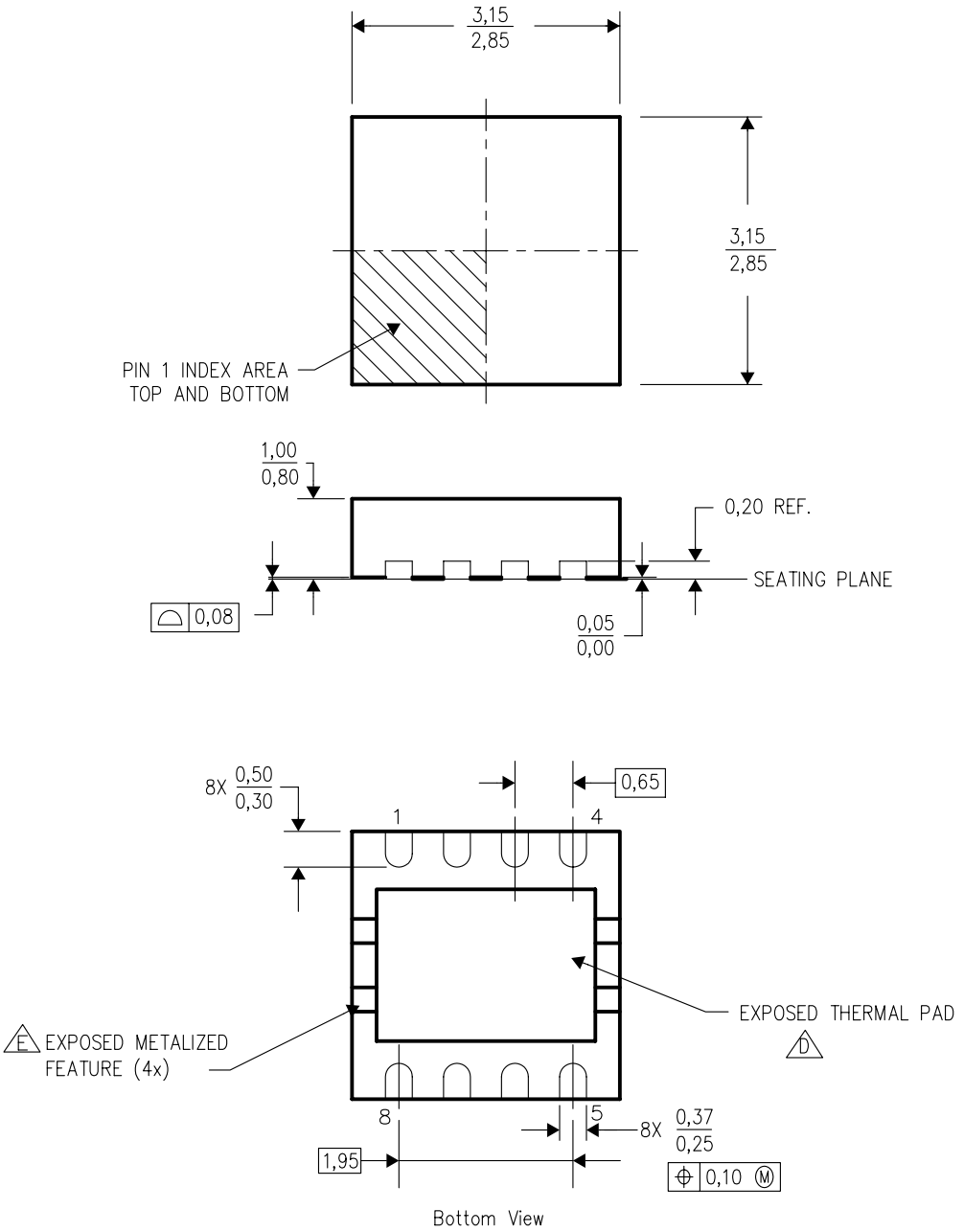
DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



4203482/G 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

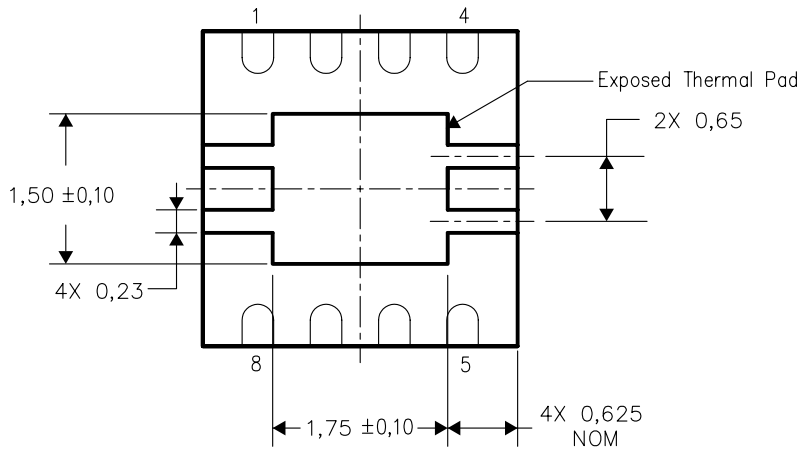
DRB (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

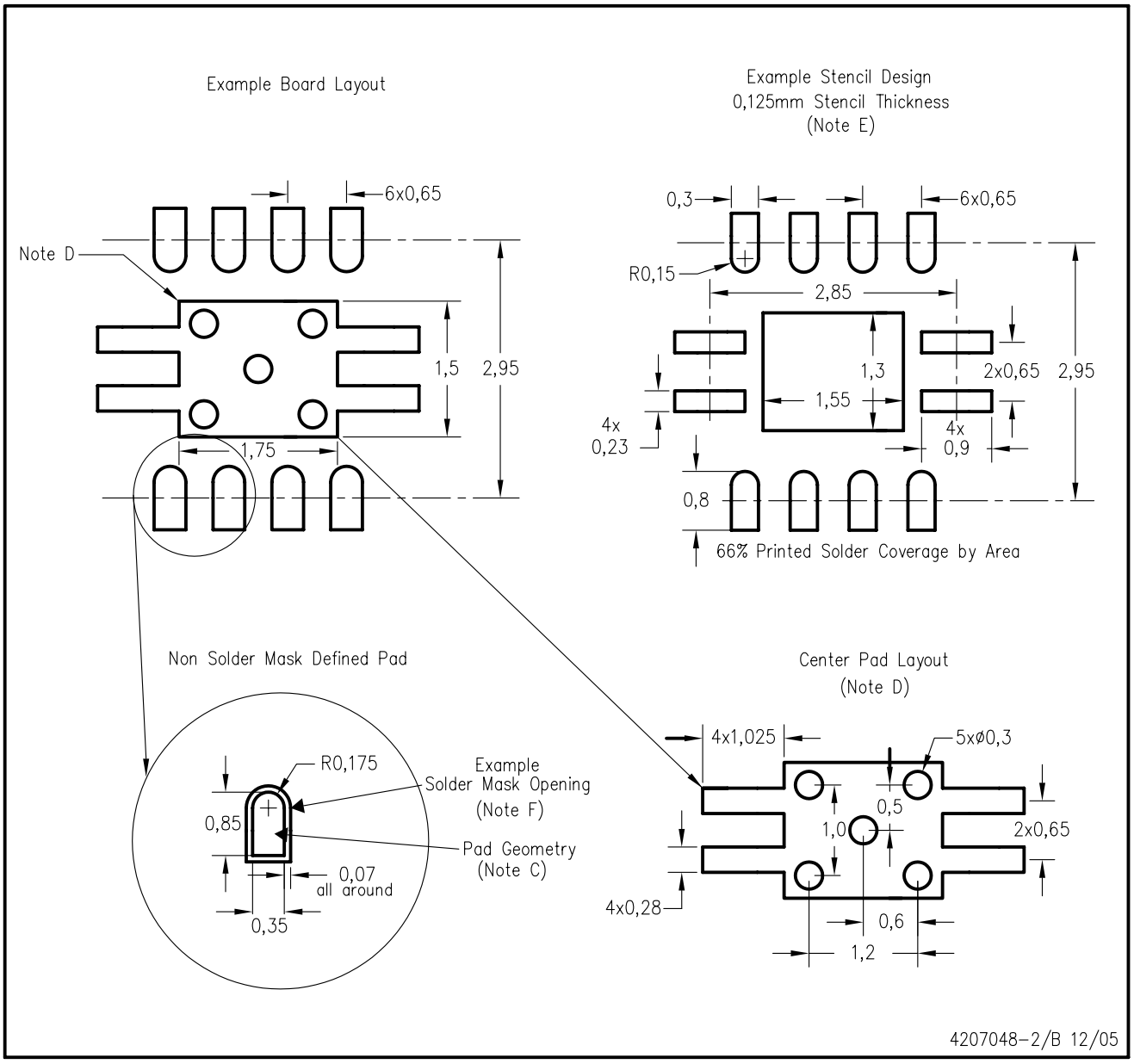


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRB (S–PDSO–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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